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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,825	11/21/2003	Donald Paul Richmond II	1008-743-301	1336

21971 7590 03/25/2008

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EXAMINER	
VAZQUEZ, ARLEEN M	
ART UNIT	PAPER NUMBER
2829	
MAIL DATE	DELIVERY MODE
03/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/718,825	RICHMOND ET AL.	
	Examiner	Art Unit	
	ARLEEN M. VAZQUEZ	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-47* is/are pending in the application.

4a) Of the above claim(s) *41-47* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-38 and 40* is/are rejected.

7)☒ Claim(s) *39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Please not that in future communications, applicants are required to provide a correct status of each claim in the Listing of the Claims. For example, the correct status of each of claims 27,29,37 and 39 submitted on 12/20/2007 should be "Currently amended" not "Previously Presented".

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 27-37 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***DeHaven et al. (US 5,701,666***) in view of ***Chong, Jr. et al. (US 6,377,471)***.

For claims 27 and 40 having the phrase of "*configured to*", applicant is reminded that claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed, or by claim language that does not limit a claim to a particular structure. The limitation of "configured to" is given patentably weight according to the doctrine of MPEP 2111.04.

As to claim 27, ***DeHaven et al.*** discloses in Figures 5-7 a system comprising a temperature controlled zone (temperature in chamber 12 is controlled by heating/cooling elements 80,82 and by temperature circuitry 50,52 in wafer 16) configured to receive a plurality of cartridges (formed by cables 20,22, connectors 24,26 and fixtures 90,92 which are holding each wafer) each containing a semiconductor wafer (14,16), power electronics (102) positioned in said cool zone (zone that is connecting system controller 104 with test fixtures 90,92 and is not receiving any application of temperature, therefore is considered as a cool zone or a zone with atmosphere temperature which is cooler than the one inside chamber 12) adjacent to said temperature controlled zone (12), a first interconnection system (test/conditioning system 104) connecting said power electronics (102), power lines (lines of Vdd and Vss of Figure 5 which are connected to/from wafers 14 and 16) coupled to the wafer (14,16) and circuitry (54,56,58,60) that measures the power lines, the measuring comprising receiving voltage measurements (from 60) or current measurements (from 56). ***DeHaven et al.*** discloses everything above but fails to teach a probe power printed circuit board making connection with power lines. However, ***Chong, Jr. et al.*** discloses in Figures 6A-6B a probe power printed circuit board (602) making connection with power lines (614 are contact lines on pcb 602 to allow electrical signals go through such as power).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify ***DeHaven et al.*** teachings by having a probe power pcb making connection with power lines as taught as ***Chong, Jr. et al.*** to provide power to

the rest of the components in the system through the electrical connections between the pcb and power lines.

As to claims 28 and 29, ***DeHaven et al.*** discloses in Figures 5-7 wherein the circuitry (54,56,58,60) compares the measurements against a programmed limit (VREF or IREF) and wherein if, according to the comparison, a measurement exceeds the limit, the circuitry shuts off power only to the respective power line that has a measurement exceeding the limit (Col. 8 ln 66- Col. 9 ln 15).

As to claims 30-33 and 37, ***DeHaven et al.*** discloses everything above but fails to teach a probe signal printed circuit board being rigid, flexible or substantially parallel to and closely spaced from the probe power printed circuit board. However, ***Chong, Jr. et al.*** discloses in Figures 6A-6B a probe signal printed circuit board (606) being rigid (is rigid enough to support other components on its surface), flexible (printed circuit boards are made of materials that have certain degree of flexibility) and is substantially parallel to and closely spaced (as shown in Figures 6A-6B) from the probe power printed circuit board (602).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify ***DeHaven et al.*** teachings by having a probe signal pcb parallel and spaced from probe power pcb as taught as ***Chong, Jr. et al.*** to avoid direct electrical contact between them but having them close enough to connect both to same components on the system.

As to claim 34, ***DeHaven et al.*** discloses in Figures 5-7 electronics (102) positioned in said cool zone (zone that is connecting system controller 104 with test fixtures 90,92 and is not receiving any application of temperature, therefore is considered as a cool zone or a zone with atmosphere temperature which is cooler than the one inside chamber 12) adjacent to said temperature controlled zone (temperature in chamber 12 is controlled by heating/cooling elements 80,82 and by temperature circuitry 50,52 in wafer 16). ***DeHaven et al.*** fails to teach a second interconnection system connecting said electronics to said probe signal printed circuit board. However, ***Chong, Jr. et al.*** discloses in Figures 6A-6B a second interconnection system (610,612) connecting said electronics (614) to said probe signal printed circuit board (606).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify ***DeHaven et al.*** teachings by having a second interconnection system connecting said electronics and the probe signal pcb as taught as ***Chong, Jr. et al.*** to allow the electronics make connection between the probe signal pcb and the rest of the components of the system different from the connection of the probe power pcb.

As to claims 35 and 36, ***DeHaven et al.*** discloses in Figures 5-7 wherein the electronics (102) are test and burn-in electronics (electronics 102 are connecting function unit 108 and analysis unit 110 will be test electronics and temperature unit 112 will be the burn-in electronics).

4. Claim 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***DeHaven et al. (US 5,701,666***) in view of ***Chong, Jr. et al. (US 6,377,471)*** further in view of ***Akram (US 6,640,323)***.

As to claim 38, the combination of ***DeHaven et al.*** in view of ***Chong, Jr. et al.*** discloses everything above but fail to teach a transition zone separating said temperature controlled and said cool zone. However, ***Akram*** discloses in Figure 4 a transition zone (190 and 194 medium which is gas) separating temperature controlled zone (burn-in test board 114) and cool zone (138, because is not receiving any hot temperature).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the combination of ***DeHaven et al.*** in view of ***Chong, Jr. et al.*** teachings by having a transition zone as taught as ***Chong, Jr. et al.*** to protect the wafers from damage of cool or hot temperatures, by exposing them suddenly to these temperatures.

Allowable Subject Matter

5. Claim 39 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 12/20/2007 have been fully considered but they are not persuasive.

7. As to argument of “It is believed that DeHaven fails to teach the claimed configuration to receive a plurality of cartridges each containing a semiconductor wafer. Instead of teaching a plurality of cartridges, DeHaven teaches a single structure formed with fixtures 90 and 92. Thus, DeHaven fails to teach a plurality of cartridges, and in fact teaches away from such approach with its single structure.”, the examiner respectfully disagrees. As clearly shown in Figure 7 of DeHaven a plurality of semiconductor wafers are disclosed, each one is received in a location formed by cables 20 and 22, connectors 24 and 26 and base formed by 90 and 92 on that specific location where each wafer is located. The physical structure for “a cartridge” is not disclosed in the claim. The only limitation for "a plurality of cartridge" is to contain a semiconductor wafer. Based on this explanations DeHaven is considered to teach “ a plurality of cartridges each containing a semiconductor wafer".

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ARLEEN M. VAZQUEZ whose telephone number is (571)272-2619. The examiner can normally be reached on Monday to Friday, 7am to 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. M. V./
Examiner, Art Unit 2829

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829